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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention	IMPROVING SYSTEMATIC YIELD IN SEMICONDUCTOR MANUFACTURE

Application Number :

Confirmation Number:

First Named Applicant: Paul Bergeron

Attorney Docket Number: BUR920040134US1

Art Unit:

Examiner:

Search string: (6341366 or 6421814 or 6430733 or 6711725 or 6189132 or 6434732 or 6260183 or 6178543 or 5636133 or 5987086 or 5923059 or 20030005401 or 20040019862).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
SW	1	6341366	2002-01-22	Wang et al.			
	2	6421814	2002-07-16	Ho			
	3	6430733	2002-08-06	Cohn et al.			
	4	6711725	2004-03-23	Rutenbar et al.			
	5	6189132	2001-02-13	Heng et al.			
	6	6434732	2002-08-13	Juengling			
	7	6260183	2001-07-10	Raspopovic et al.			
	8	6178543	2001-01-23	Chen et al.			
	9	5636133	1997-06-03	Chesebro et al.			
	10	5987086	1999-11-16	Raman et al.			
	11	5923059	1999-07-13	Gheewala			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
SW	1	20030005401	2003-01-02	Wimer			
SW	2	20040019862	2004-01-29	Li et al.			

Signature /Stacy Whitmore/   01/22/2007

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
							☐	☐

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

SW			R.L. Hunt, et al., "Automatically Rerouting Wires on Printed-Circuit Boards to Avoid Noise Coupling Problems", IBM Technical Disclosure Bulletin, Vol. 18, No. 3, August 1975, p. 762-766.
SW			J.Z. Su, et al., "Post-Route Optimization for Improved Yield Using a Rubber-Band Wiring Model", Computer Aided Design, 1997. Digest of Technical Papers., 1997. IEEE/ACM International Conference on Nov. 9-13, 1997, p. 700-706.
SW			R. Prasad, et al., "The Effect of Placement on Yield for Standard Cell Designs", url = "citeseer.ist.psu.edu/380923.html"
SW			A.B. Kahng, et al., "Non-Tree Routing for Reliability and Yield Improvement", Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on Nov. 10-14, 2002, p. 260-266.
SW			A. Venkataraman, et al., "Determination of Yield Bounds Prior to Routing", Defect and Fault Tolerance in VLSI Systems, 1999. DFT '99. International Symposium on Nov. 1999, p. 4-13.
SW			P. Kudva, et al., "Measurements for Structural Logic Synthesis", Computer Aided Design of Integrated Circuits and Systems, IEEE Transactions on Vol. 22, Iss. 6, June 2003, p. 665-674.

EXAMINER	/Stacy Whitmore/	DATE CONSIDERED	01/22/2007